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10/581,849	10/16/2007	Gunther Leising	U 016328-0	4589

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EXAMINER	
TAVLYKAEV, ROBERT FUATOVICH	
ART UNIT	PAPER NUMBER
4116	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/581,849	LEISING ET AL.	
	Examiner	Art Unit	
	ROBERT TAVLYKAEV	4116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16,21-23,26-28,30,32 and 34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16,21-23,26-28,30,32 and 34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/16/07, 5/19/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the Preliminary Amendment filed October 16, 2007, Claims 17-20, 24, 25, 29, 31, 33 and 35-37 have been cancelled and claims 1-16, 21-23, 26-28, 30, 32 and 34 are pending.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-16, 21-23, 26-28, 30, 32 and 34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding to claims 1-16, 21-23, 26-28, 30, 32 and 34, the reference numbers in the claims are inconsistency with each other, *inter alia*, claim 3 refers to the optical layer (3, 3') but claim 1 has only an optical layer (3); claim 10 refers to the optoelectronic component (4, 5) and claim 1 only has an optoelectronic component (4, 5; 4', 5'). More instances of discrepancy in using numerals are found throughout the claims. For the purposes of this Action, all numerals are disregarded. Appropriate correction is required.

In claim 3, the phrase "for instance" renders the claim indefinite because it is unclear as to what are the metes and bounds for the claimed limitation set forth in the claim. See MPEP § 2173.05(d). For the purposes of this Action, the fragment " … formed, for instance, by two plies" is disregarded.

Claim 8 cites "… electronic component to an embedded unit". There appears to be a missing word(s). For the purposes of this Action, this fragment is interpreted as electronic component to form an embedded unit.

In claim 16, the acronym "e. g." renders the claim indefinite because it is unclear whether the limitation(s) following the acronym are part of the claimed invention. See MPEP § 2173.05(d). For the purposes of this Action, the fragment " e.g. with an arc-shaped transition …" is disregarded.

Claim 12 recites the limitation "in the substrate" in the last line. There is insufficient antecedent basis for this limitation in the claim. For the purposes of this Action, the limitation is interpreted as – in a substrate.

Claim 13 recites the limitation "the electrically insulating optical layer" in the last line. There is insufficient antecedent basis for this limitation in the claim. For the purposes of this Action, the limitation is interpreted as – an electrically insulating optical layer.

Claims 16, 23, 28, 30, 32, and 34 have the same word pattern "at least one of characterized ..." followed by at least two alternatives, each of those formulated by a relatively long word sequence that contains nouns and verbs. By condensing several claims into one with the others cancelled, the applicant has produced claims unintelligible to a person of ordinary skill in the art. For the purposes of this Action, the above claims are interpreted as Markush-type clams with the corresponding original claims included as alternatives. Appropriate correction of the claim language is required.

In claims 21-23, 26-28, 30, 32 and 34, the preamble is misdescriptive, because the preamble is directed to the method and depended on claim 1 which is directed to the apparatus,

printed circuit board elements. In addition, claim 28 cites "... combined to a unit". There appears to be a missing word(s). For the purposes of this Action, this fragment is interpreted as combined to form a unit. Further, claim 30 refers to a cancelled claim 29. For the purposes of this Action, the claim is interpreted as referring to claim 28.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-7, and 10-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Iwaki et al (US Pub. No. 2004/0001661 A1).

Regarding claim 1, Fig. 1 of Iwaki et al discloses a printed circuit board element including at least one optical waveguide (105) provided in an optical layer (104) and at least one optoelectronic component (103) in optical connection with the optical waveguide (105), characterized in that the optoelectronic component (103) is embedded in the optical layer (104), that the optical waveguide (105) adjoins the optoelectronic component (103), and that the optical waveguide is structured by irradiation (see paragraph [0048] and [0054]) within the optical layer (104).

Regarding claim 2, Fig. 6 and 1 show that the optoelectronic component (103) with one side may border upon a substrate (129b) carrying the optical layer (104), or a cladding layer (106) applied thereon, respectively. It is obvious that the board element in Fig. 1 may have a substrate disposed similarly to the substrate (129b) in Fig. 6 in order to increase the mechanical stability/rigidity of the board element (see paragraph [0059] of Iwaki).

Regarding claim 3, the optoelectronic component (103) in Fig. 1 is embedded in the optical layer (104) on all sides.

Regarding claim 4, the optical layer (104) in Fig. 1 may be realized as a flexible layer, such as a polymer layer (see paragraph [0053]).

Regarding claim 5, Fig. 1 shows two optoelectronic components ((103) and (101)), connected with each other via the optical waveguide (105), are embedded in the optical layer (104).

Regarding claims 6 and 7, the optoelectronic component (103) in Fig. 2 borders upon a heat-dissipation layer (121c) connected to a heat-sink part (125). The heat-dissipation layer (121c) is formed by a patterned inner ply (see Fig. 7B).

Regarding claims 10-12, the optoelectronic component (103) in Fig. 6 borders on an electrically conductive distribution layer (to the left from the part 121a), the latter being connected with an external contact (141) through a via (140) provided in a substrate (129a) that carries the optical layer (104).

Regarding claims 13 and 14, Fig. 6 shows a printed circuit board layer ((129a) or (129b)) having a patterned, conductive inner ply (comprising the part (121a)) and/or outer ply (comprising the part (141) or the 2 electrically conductive parts on the bottom surface on the

layer (129b)) is applied on at least one side of an electrically insulating optical layer (104). Furthermore, the optoelectronic component (103) is contacted through vias (part (140) and the next one to the right) provided in the printed circuit layer (129a). Fig. 2 shows a contact to the optoelectronic component (103) made through a via (125) in the optical layer (104).

Regarding claim 15, Fig. 8 shows an electronic component (113) connected with the optoelectronic component (103). Iwaki further teaches (see paragraph [0085]) that there may be a printed circuit board layer placed between the electronic component (113) and the optical layer (104). Fig.6 explicitly shows at least one such printed circuit board layer (parts (129a) and (129b)), to which the electronic component (113) would be mounted to.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 16, 21-23, 26, 27 and 34 as best understood are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwaki et al (US Pub. No. 2004/0001661 A1).

Regarding claims 16 and 34, Fig. 15 of Iwaki discloses an optical waveguide (105) provided with a lens structure (109) on its end adjacent an optoelectronic component (101), the latter being a light reception device. The lens structure at least partially encloses the optoelectronic component (101) and is used for focusing light into the optoelectronic component (101). The focusing property depends on the refractive index of the material used to form the lens structure (109). Iwaki et al do not explicitly state that the lens structure (109) can be made a part of the optical waveguide (105). However, Iwaki et al do cite (see paragraph [0098]) that the refractive index of the material should be higher than that of the optical layer (104). Thus, it would have been obvious to a person of ordinary skill in the art that the material of the optical waveguide (105) can be used to from the lens structure (109), since the refractive index of optical waveguide (105) satisfies the above condition. The motivation for forming the lens structure (109) as a part of the optical waveguide (105) is that such a structure would have a

reduced the number of needed materials, can be produced in a single step, and reduces cost, while still providing the benefit of an improved light collection efficiency.

Regarding claim 21, Figs. 7A – 7I show steps of a method for producing a printed circuit board element, for example, one shown in Fig. 2, that has all the limitations of claim 1 (see argument for claim 1 above) and some additional features. Furthermore, the disclosed method has all of the steps of claim 21 as well as additional steps. In particular, the disclosed method produces a printed circuit board element having recesses to be filled with a light transmitting resin (109)(see paragraph [0055]). Iwaki et al do not explicitly illustrate a method for producing a printed circuit board element without recesses, such as that shown in Fig. 1. However, it would have been obvious to a person of ordinary skill in the art that the printed circuit board element shown in Fig.1 can be produced using the following sequence: (a) the step shown in Fig. 7D, which illustrates a step of mounting at least one optoelectronic component, e.g., (103) to a substrate (119); (b) the step shown in Fig. 7B, which illustrates a step of applying an optical layer (104) to the substrate (119), the optical layer being comprised of an optical material changing its refractive index upon photon irradiation. Without the recesses shown in Fig. 7b and the optoelectronic component (103) already mounted to a substrate (119), the optical layer (104) would embed the optoelectronic component (103); (c) the step shown in Fig. 7A, which illustrates a step of producing, by photon irradiation, a waveguide structure (105) in the optical layer (104) in order to adjoin the optoelectronic component (103). The motivation for using a method with such step sequence is that it is a simplest and shortest sequence that can be used to produce the printed circuit board element shown in Fig. 1 of Iwaki et al. Therefore, production cost can be reduced, since the additional steps, which are shown in Figs. 7A – 7I and needed for

the more complicated printed circuit board element shown in Fig. 2, would be superfluous for the printed circuit board element shown in Fig. 1.

Regarding claim 22, Fig. 1 shows two optoelectronic components (i.e., parts (101) and (103)), which are embedded in the optical layer (104) and thereafter are connected with each another by the optical waveguide (105) directly adjoining the same. It would have been obvious to a person of ordinary skill in the art that the board element in Fig. 1 may have a substrate, which is used for mounting the two optoelectronic components and disposed similarly to the substrate (129a) in Fig. 6, in order to increase the mechanical stability / rigidity of the board element (see paragraph [0059] of Iwaki).

Regarding claim 23, Fig. 7B shows that after the production of the optical waveguide structure (105) in the optical layer (104), a printed circuit board layer (119) including a conductive inner ply (comprising the parts (121a) and (121c)) is applied to at least one side of the optical layer (104).

Regarding claim 26, Fig. 6 shows that vias (140) are provided in the optical layer (104) and also in the printed circuit board layer (129a), in coordination with the respective optoelectronic component (103) and that electrically conductive connections to the optoelectronic component are established through the vias.

Regarding claim 27, Fig. 8 shows that the optoelectronic component (103) is conductively connected with an associated electronic component, i.e. a driving part (113). Fig. 8 does not explicitly show a printed circuit layer or a substrate. However, it would have been obvious to a person of ordinary skill in the art that there may be a printed circuit layer (which is included between the part (113) and the optical layer (104) and is used for mounting the part

(113)), because Iwaki et al illustrate such a printed circuit layer in Fig. 6 and teach that this arrangement is desirable as providing increased mechanical stability/rigidity of the entire printed circuit board element (see paragraph [0059] of Iwaki).

9. Claims 8, 9, 28, 30 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwaki et al (US Pub. No. 2004/0001661 A1) in view of Yoshimura et al (US Patent No. 6,684,007 B2) .

In regard to claims 8, 9 and 28, Fig. 8 of Iwaki shows that the optoelectronic component (103) is used with an associated electronic component, i.e. a driving component (113). In Fig. 8, the driving component (113) is shown to be positioned on one side of the board. However, Iwaki's invention also includes an embodiment, wherein the driving device (113) is arranged inside the board (see paragraph 85), thus making it an embedded unit. The optoelectronic component (103)(e.g., a light emission device (see paragraph [0046])), if combined with the driving component (113)(i.e. an electronic driver), is an optoelectronic chip. Therefore, Iwaki et al teach all of the subject matter, except for stating that the optoelectronic component (103) may be combined to form a unit with an associate electronic component (113)(shown in Figs. 6 and 8). Yoshimura et al disclose a printed circuit board element, which may have a polymer optical waveguide, electrical layers, and vias, and teach (see col. 62, lines 28-66) that a VCSEL (optoelectronic device) with an integrated driver (electronic component) or a photodetector (optoelectronic device) with an integrated amplifier (electronic component) may also be used. Thus, it would also have been obvious to a person of ordinary skill in the art that the optoelectronic component (103), which is embedded in the optical layer (104) and mounted to a

substrate, as disclosed by Iwaki, can be combined to form an optoelectronic chip unit with an associate electronic component, as disclosed by Yoshimura et al. The motivation is that a smaller footprint and higher component packing density can be realized by such integration, compared to using individual components.

Regarding claim 30, Iwaki et al teach (see paragraph [0085]) that the disclosed printed circuit board element can include multilayer boards on one of both sides of the optical layer. Two or more layers in a multilayer board represent a cladding layer and a substrate. Iwaki et al further teach (see paragraph [0065]) that some layers can be made of a light blocking material. It would also have been obvious to a person of ordinary skill in the art that if a substrate layer is made of a light blocking material, then a cladding/buffer layer would be required between the substrate and the optical layer, in order to avoid high optical loss in the optical layer. The motivation for such a substrate / cladding layer combination is that both low-loss optical transmission and reduced optical cross-talk due to suppressed stray light (see paragraph [0065]) can be obtained.

Regarding claim 32, Fig. 6 shows that electrical connections for the optoelectronic components (103) and (101) are established throughout an electrically conductive distribution layer (comprising parts (121a) and (121c)), which is also configured as a heat-dissipation layer.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Oda et al (US Patent No. 6,477,284 B1) disclose an optoelectronic board comprising an optical waveguide, optoelectronic components, and electrical connections including vias.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT TAVLYKAEV whose telephone number is (571)270-5634. The examiner can normally be reached on Mon - Thur 8 am - 5 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joe Cheng can be reached on 571-272-3171. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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7/15/08

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